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DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 1 of 15

FIG. 1A (PRIOR ART)

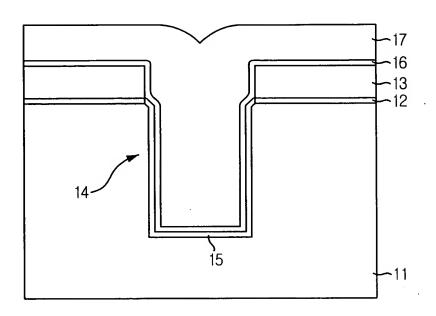
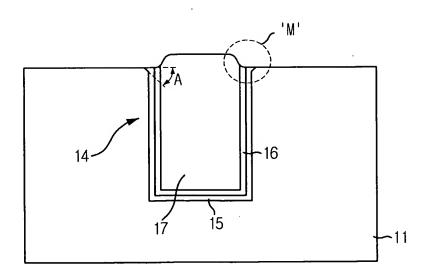


FIG. 1B (PRIOR ART)



DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 2 of 15

FIG. 2A

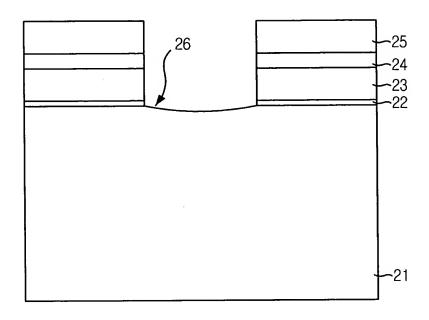
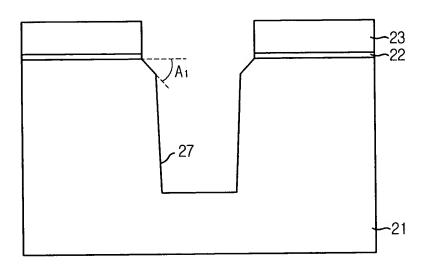


FIG. 2B



DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 3 of 15

FIG. 2C

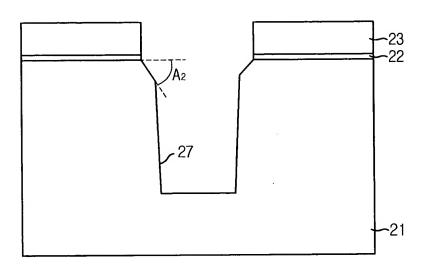
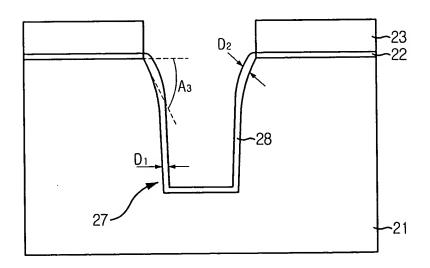


FIG. 2D

 $D_2 > D_1$ 



Blakely, Sokoloff, Taylor & Zafman LLP

(310) 207-3800

Title: METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING TRENCH TYPE

DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US

Sheet: 4 of 15

FIG. 2E

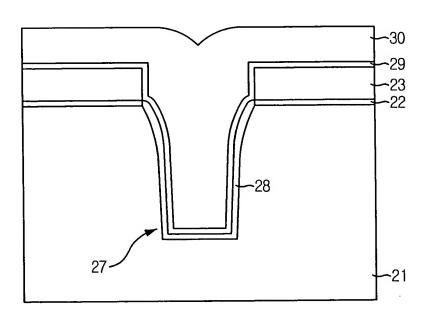
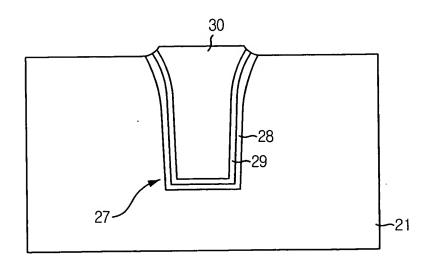


FIG. 2F



DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG
Express Mail No.: EV339912681US
Sheet: 5 of 15

FIG. 2G

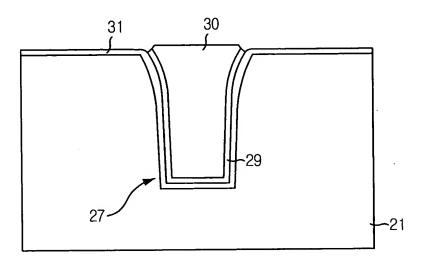
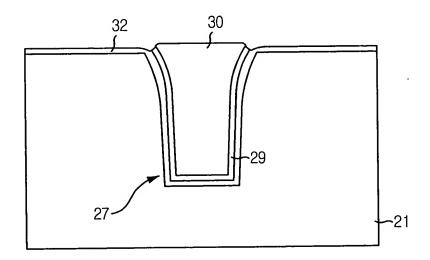


FIG. 2H



DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US

Sheet: 6 of 15

FIG. 3A

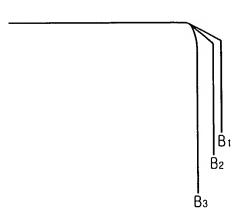
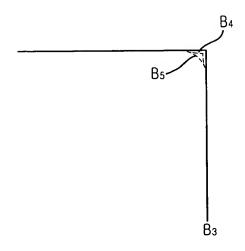


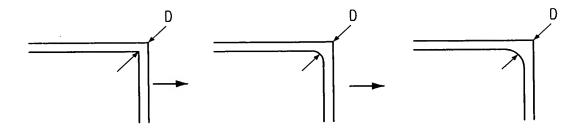
FIG. 3B



DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 7 of 15

FIG. 3C



1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 8 of 15

FIG. 4A

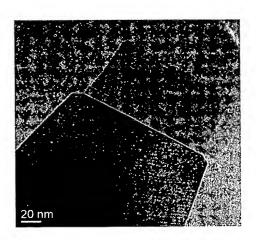
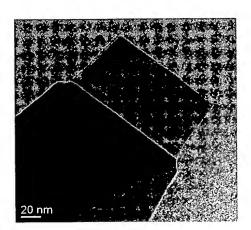


FIG. 4B



DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG
Express Mail No.: EV339912681US
Sheet: 9 of 15

FIG. 4C

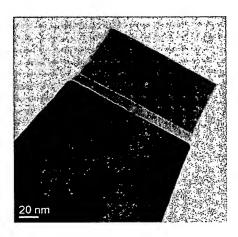
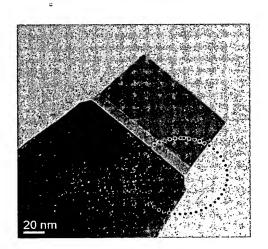


FIG. 5A



Docket No.: 51876P542

DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 10 of 15

FIG. 5B

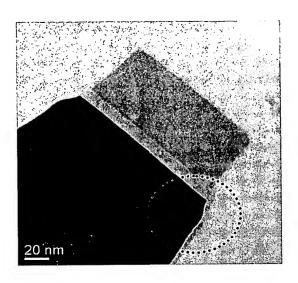
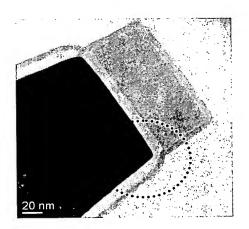
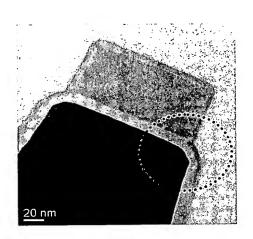


FIG. 5C



Brakely, Sokoloff, Taylor & Zafman LLP (310) 207-3800
Title: AMETHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING TRENCH TYPE
DEVICE ISOLATION LAYER
1st Named Anyentor: Tae-Woo JUNG
Express Mail No.: EV339912681US
Docket No.: 51876P542
Sheet: 11 of 15

도 5D



Docket No.: 51876P542

DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 12 of 15

FIG. 6A

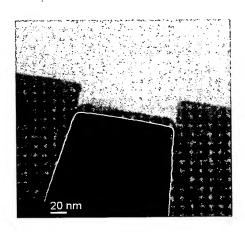
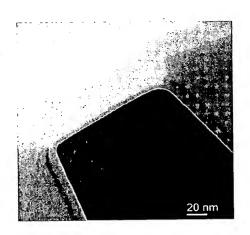


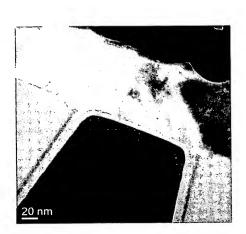
FIG. 6B



DEVICE ISOLATION LAYER
1st Named Inventor: Tae-Woo JUNG
Express Mail No.: EV339912681US
Sheet: 13 of 15

Docket No.: 51876P542

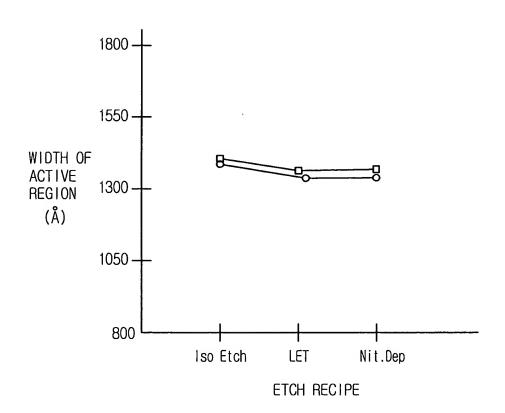
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DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US Sheet: 14 f 15

FIG. 7



(310) 207-3800

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Title: METHOD FOR FABRICATING SEMICONDUCTOR DEVICE HAVING TRENCH TYPE

DEVICE ISOLATION LAYER

1st Named Inventor: Tae-Woo JUNG Express Mail No.: EV339912681US

Sheet: 15 of 15

FIG. 8

